EPA/EPO/OEB
D-80298 München
+49 89 2399-0
TX 523 656 epmu d
FAX +49 89 2399-4465

Europäisches Patentamt | European Patent Office | Office européen des brevets

Generaldirektion 2 | Directorate General 2 | Direction Générale 2

Telephone numbers: Branch at The Hague
Primary Examiner (substantive examination) +31 70 340-2983
Formalities Officer / Assistant (Formalities and other matters) +31 70 340-2264

Hutchinson, Glenn Stanley
Harrison Goddard Foote,
Fountain Precinct
Balm Green
Sheffield S1 2JA
ROYAUME-UNI

Application No.	Ref.	Date
98 930 171.8 - 1235	P71376EP	27.02.2004
Applicant: The Regents of The University of California		

Communication pursuant to Article 96(2) EPC

The examination of the above-identified application has revealed that it does not meet the requirements of the European Patent Convention for the reasons enclosed herewith. If the deficiencies indicated are not rectified the application may be refused pursuant to Article 97(1) EPC.

You are invited to file your observations and insofar as the deficiencies are such as to be rectifiable, to correct the indicated deficiencies within a period

of 4 months

from the notification of this communication, this period being computed in accordance with Rules 78(2) and 83(2) and (4) EPC.

One set of amendments to the description, claims and drawings is to be filed within the said period on separate sheets (Rule 36(1) EPC).

Failure to comply with this invitation in due time will result in the application being deemed to be withdrawn (Article 96(3) EPC).

EUROPÄISCHES PATENTAMT - EUROPEAN PATENT OFFICE - OFFICE EUROPÉEN DES BREVETS

GORI P
Primary Examiner
for the Examining Division

Enclosure(s): 3 page/s reasons (Form 2906)

Registered Letter
EPO Form 2001 07.02CSX

The examination is being carried out on the **following application documents:**

Text for the Contracting States:
DE FR NL

Description, pages:

1-18 as published

Claims, No.:

1-22 as published

Drawings, sheets:

1/13-13/13 as published

****

1. The following documents are referred to in this communication; the numbering will be adhered to in the rest of the procedure :

D1 : US-A-5 627 317;
D2 : WO-A-9508775;

2. Document D1 discloses, see the figures and the detailed description, a process for forming an acceleration sensor comprising :
- providing a SOI wafer, composed of a handle wafer (4), an oxide layer (3) and a device layer (2), see also col. 1, lines 48-55,
- etching a trench (15) surrounding (col. 2, lines 13-17) a first region in the device layer, and filling said trench with an insulating material (col. 3, lines 6-16) and
- etching a second trench in the device layer in the first region, said second trench defining a movable electrode, see the figures.

The process also provides for interconnections over the trench (16) to make contact with different regions of the wafer, and the movable electrode (10) is obtained by undercutting the oxide layer of the SOI (sentence bridging columns 2 and 3) after having etched the trenches up to said oxide.

Consequently the subject matter of claims 1-10, 13-20 is entirely known from D1. These claims are thus not allowable under Art. 54 EPC.

3. Should the subject matter of claim 2 to be understood as meaning that "circuitry" in the form of electronic devices, transistors, diodes etc... are formed in the substrate, it is noted that these features are not directly shown by D1. However there can be no doubt that in the context of a capacitive sensor (fixed electrodes and seismic mass) the formation on the same substrate of the necessary amplifiers, buffers and detection circuits will be considered as beneficial by the skilled person. This claim, possibly clarified, cannot support an inventive activity (Art. 56 EPC).

4. The subject matter of claims 11, 12, 21 and 22 is considered well known to the skilled person in the art of SOIs or microstructures. These claims cannot be considered as involving an inventive step (Art. 56 EPC), even in the frame of combinations of the above claims.

5. Document D2 discloses, see the figures and page 5, line 15 to page 12, line 26, a process which is prejudicial to the novelty of claims 1, 2, 4-11, 13-16, 18-21 (Art. 54 EPC). Additionally the document emphasizes on the compatibility of the disclosed process with standard VLSI process, so that there is no doubt that the interconnections represented on Fig. 5a and 6 can be made with the classical VLSI process, i.e. over the isolation trenches. Thus the subject matter of claims 3 and 17 is considered anticipated.

The claims 12 and 22 are considered not inventive, see above.

6. It is not at present apparent which part of the application could serve as a basis for a new, allowable claim. Indeed after having carefully reviewed the whole application it appears that no combination of claims would be allowable under Art. 54 and/or 56 EPC. In the same manner the description does not contain features which would allow

to envisage a positive prosecution of the application. Independently of the above it is noted that the term "microstructure" is extremely vague. While considering that a trench (topographic feature of a micronic size) is a microstructure, the subject matter of the claims is anticipated by the whole available art relating to trench isolation of electronic devices. Should the applicant wish to further prosecute it would then be necessary to bring a minimum of limitations to the subject matter of the claims.

However the opinion of the examining division is such that the applicant is asked to take into account a rapid rejection of the application under Art. 97(1) EPC.